Lecture Notes

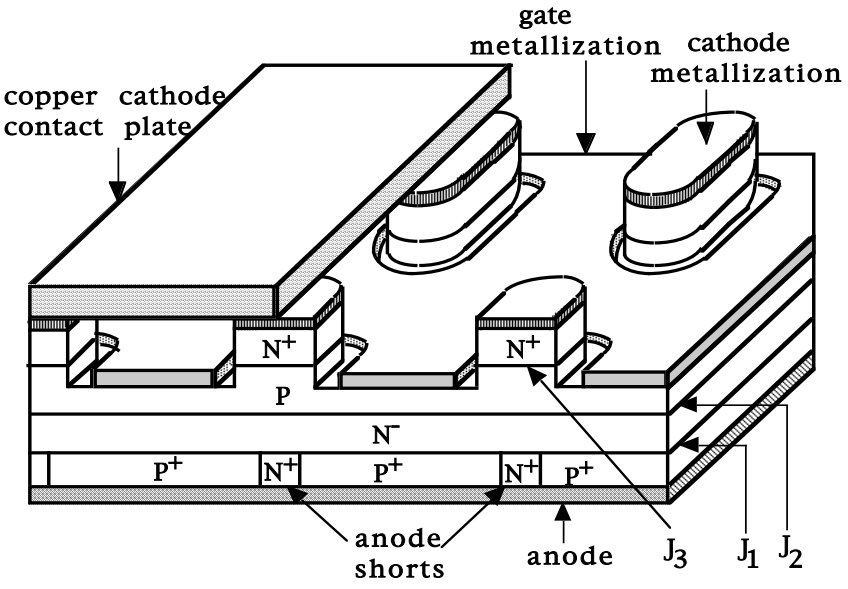
Gate Turn-off Thyristors (GTOS)

OUTLINE

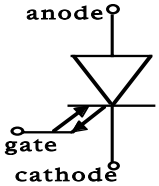
- GTO construction and I-V characteristics.
- Physical operation of GTOs.
- Switching behavior of GTOS

GTO (Gate Turn-off Thyristor) Construction

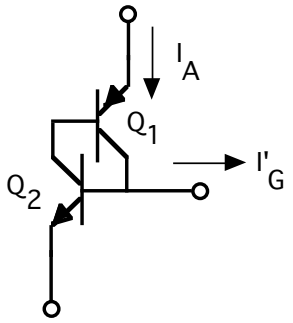
- Unique features of the GTO.
  - Highly interdigitated gate-cathode structure (faster switching)
  - Etched cathode islands (simplify electrical contacts)
  - Anode shorts (speed up turn-off)
- GTO has no reverse blocking capability because of anode shorts
- Otherwise i-v characteristic the same as for standard SCR



GTO circuit symbol



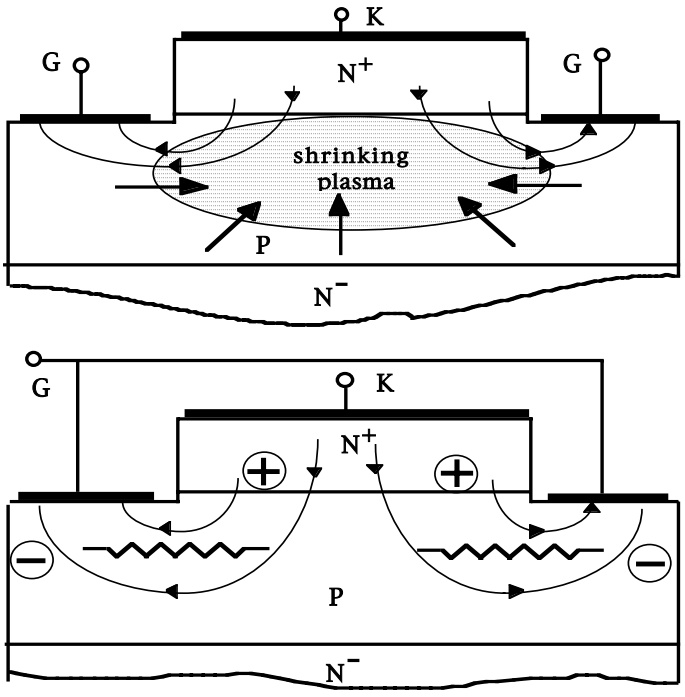
GTO Turn-off Gain



- Turn off GTO by pulling one or both of the BJTs out of saturation and into active region.
- Force Q_2 active by using negative base current I_G' to make $I_{B2} < \frac{I_{C2}}{\beta_2}$
- $I_{B2} = \alpha_1 I_A - I'_G \quad ; \quad I_{C2} = (1 - \alpha_1) I_A$
- $\alpha_1 I_A - I'_G < \frac{(1 - \alpha_1) I_A}{\beta_2} = \frac{(1 - \alpha_1)(1 - \alpha_2) I_A}{\alpha_2}$
- $I'_G < \frac{I_A}{\beta_{off}}$; $\beta_{off} = \frac{\alpha_2}{(1 - \alpha_1 - \alpha_2)}$ = turn-off gain

- Large turn-off gain requires $\alpha_2 \approx 1$, $\alpha_1 << 1$
- Make α_1 small by
  1. Wide n_1 region (base of Q_1) - also needed for large blocking voltage
  2. Short lifetime in n_1 region to remove excess carriers rapidly so Q_1 can turn off
- Short lifetime causes higher on-state losses
- Anode shorts helps resolve lifetime delimma
  1. Reduce lifetime only moderately to keep on-state losses reasonable
  2. N^+ anode regions provide a sink for excess holes - reduces turn-off time
- Make $\alpha_2 \approx$ unity by making p_2 layer relatively thin and doping in n_2 region heavily (same basic steps used in making beta large in BJTs).
- Use highly interdigitated gate-cathode geometry to minimize cathode current crowding and di/dt limitations.

Maximum Controllable Anode Current



- Large negative gate current creates lateral voltage drops which must be kept smaller than breakdown voltage of J_3.
- If J_3 breaks down, it will happen at gate-cathode periphery and all gate current will flow there and not sweep out any excess carriers as required to turn-off GTO.
- Thus keep gate current less than $I_{G,max}$ and so anode current restricted by $I_A < \frac{I_{G,max}}{\beta_{off}}$

GTO Step-down Converter

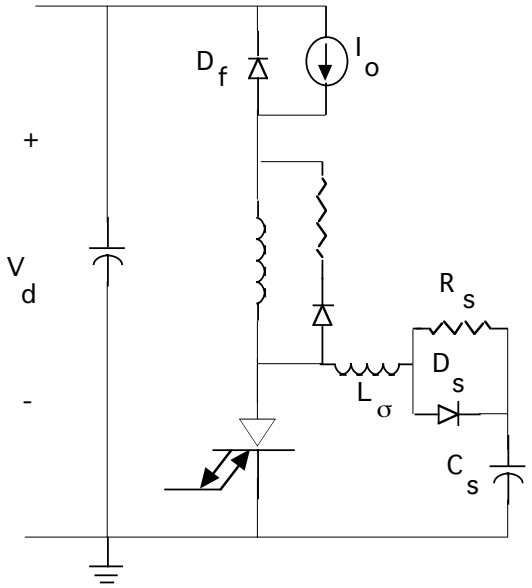
- GTO used in medium-to-high power applications where electrical stresses are large and where other solid state devices used with GTOs are slow e.g. free-wheeling diode D_F.

- GTO almost always used with turn-on and turn-off snubbers.

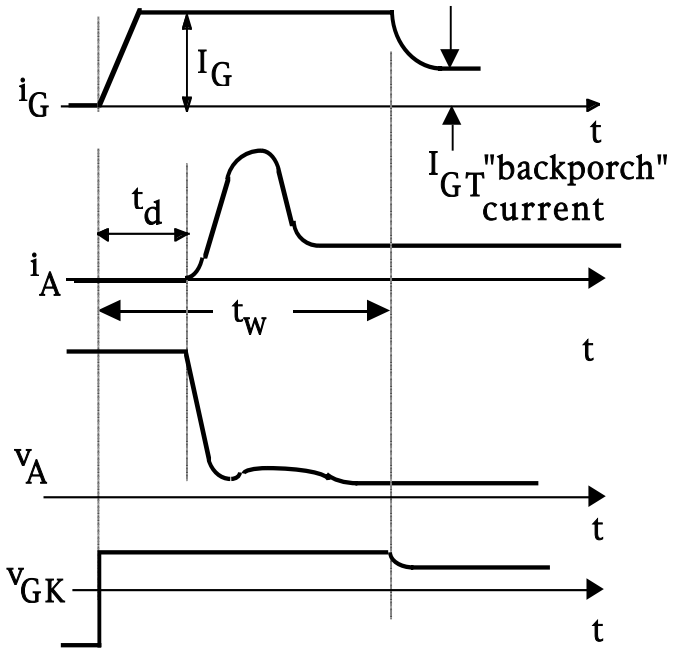
  1. Turn-on snubber to limit overcurrent from D_F reverse recovery.

  2. Turn-off snubber to limit rate-of-rise of voltage to avoid retriggering the GTO into the on-state.

- Hence should describe transient behavior of GTO in circuit with snubbers.



GTO Turn-on Waveforms



- GTO turn on essentially the same as for a standard thyristor

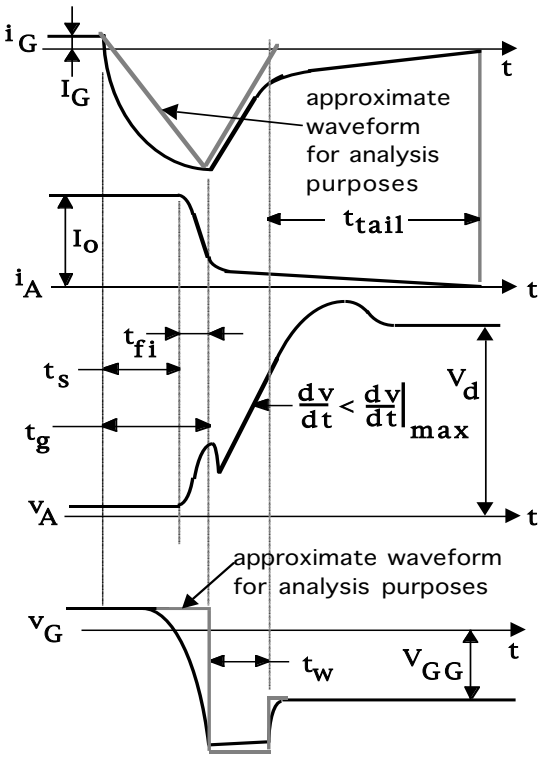
- Large I_{GM} and large rate-of-rise insure all cathode islands turn on together and have good current sharing.

- Backporch current I_{GT} needed to insure all cathode islands stay in conduction during entire on-time interval.

- Anode current overshoot caused by free-wheeling diode reverse recovery current.

- Anode-cathode voltage drops precipitiously because of turn-on snubber

GTO Turn-off Waveforms



- t_s interval

  Time required to remove sufficient stored charge to bring BJTs into active region and break latch condition

- t_{fi} interval

  1. Anode current falls rapidly as load current commutates to turn-off snubber capacitor
  2. Rapid rise in anode-cathode voltage due to stray inductance in turn-off snubber circuit

- t_{w2} interval

  1. Junction J_3 goes into avalanche breakdown because of inductance in trigger circuit. Permits negative gate current to continuing flowing and sweeping out charge from p_2 layer.
  2. Reduction in gate current with time means rate of anode current commutation to snubber capacitor slows. Start of anode current tail.

- t_{tail} interval

  1. Junction J_3 blocking, so anode current = negative gate current. Long tailing time required to remove remaining stored charge.
  2. Anode-cathode voltage growth governed by turn-off snubber.
  3. Most power dissipation occurs during tailing time.

Lecture Notes

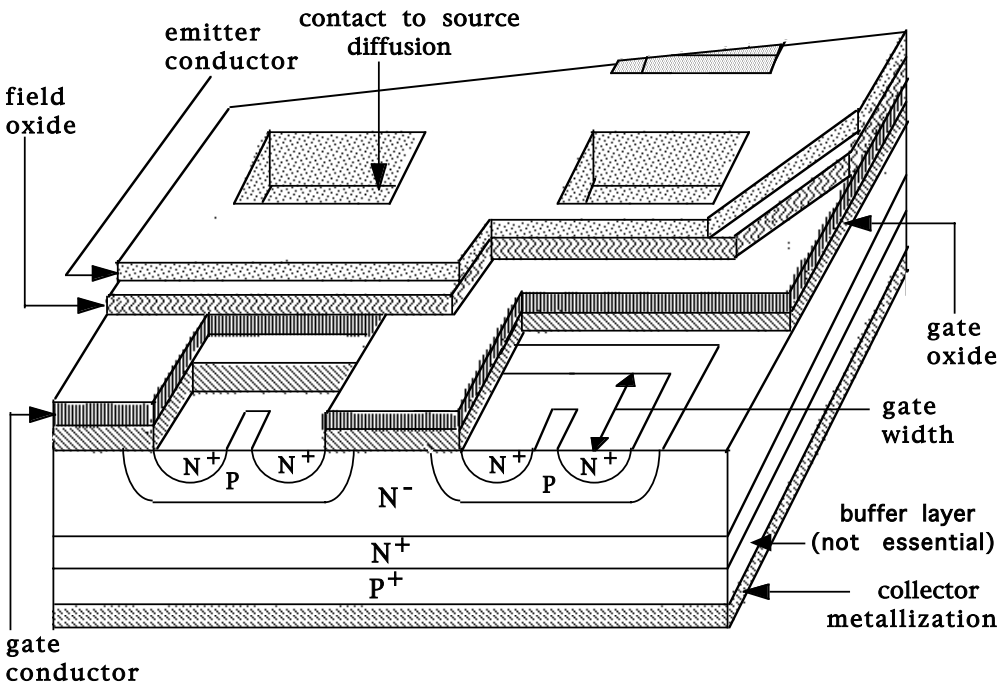
Insulated Gate Bipolar Transistors (IGBTs)

Outline

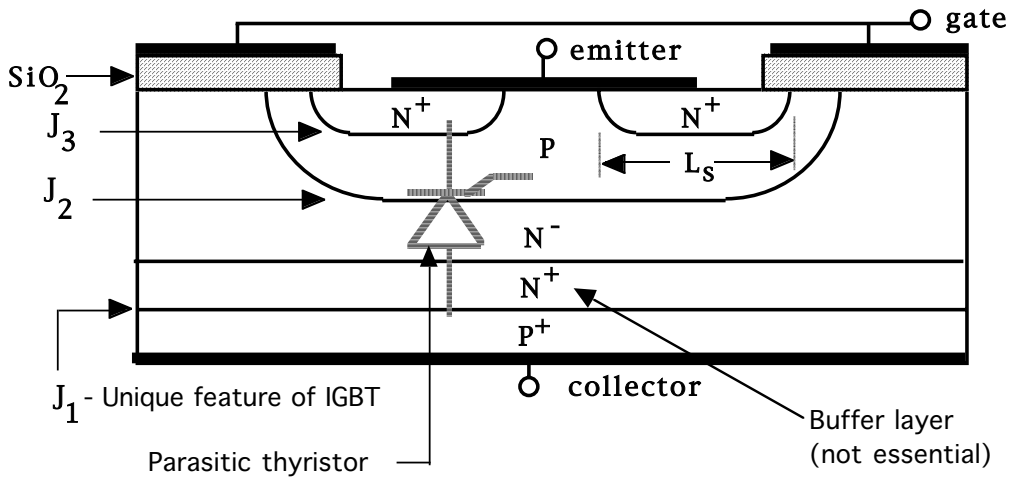
- Construction and I-V characteristics
- Physical operation
- Switching characteristics
- Limitations and safe operating area
- PSPICE simulation models

Multi-cell Structure of IGBT

- IGBT = insulated gate bipolar transistor.

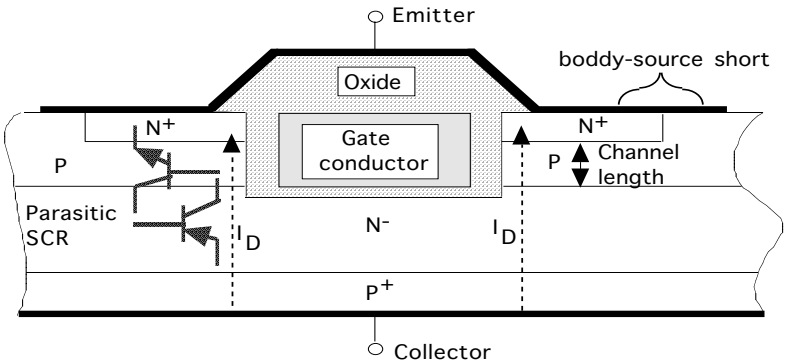


Cross-section of IGBT Cell

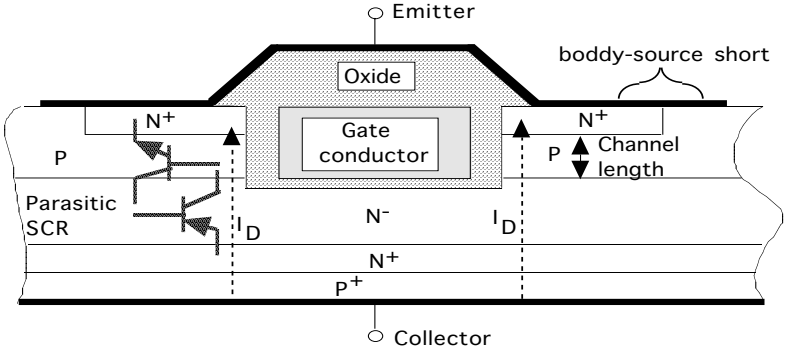


- Cell structure similar to power MOSFET (VDMOS) cell.
- P-region at collector end unique feature of IGBT compared to MOSFET.
- Punch-through (PT) IGBT - N^+ buffer layer present.
- Non-punch-through (NPT) IGBT - N^+ buffer layer absent.

Cross-section of Trench-Gate IGBT Unit Cell

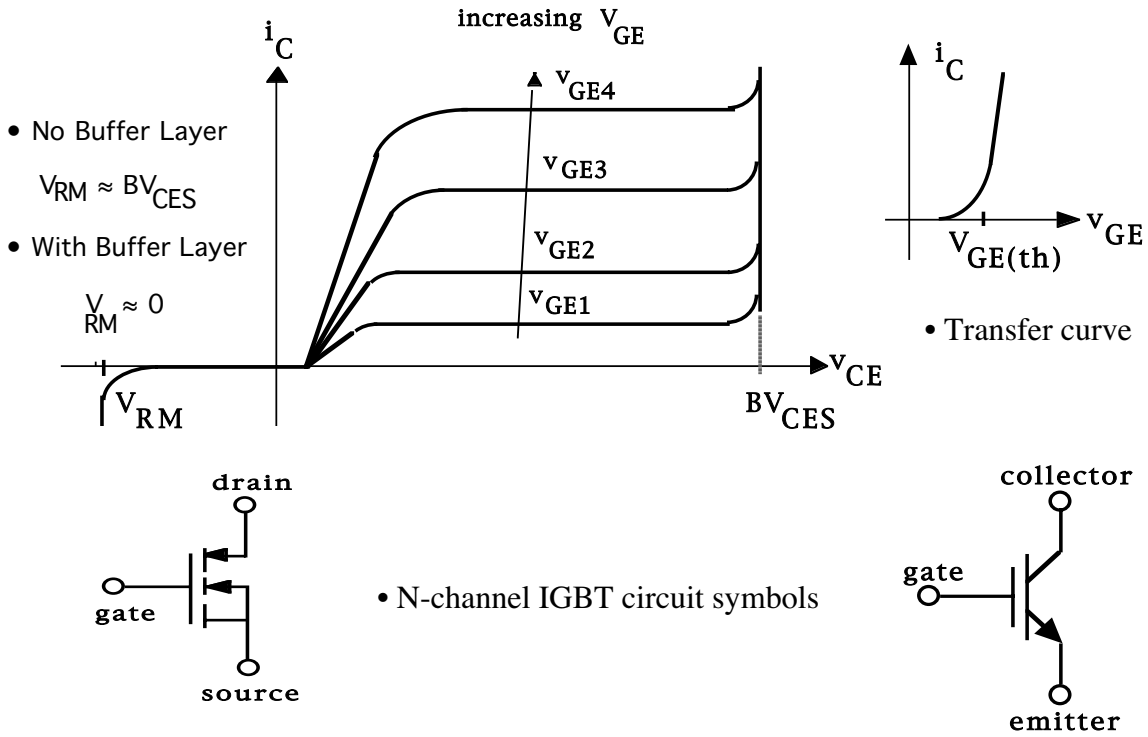


- Non-punch-thru IGBT

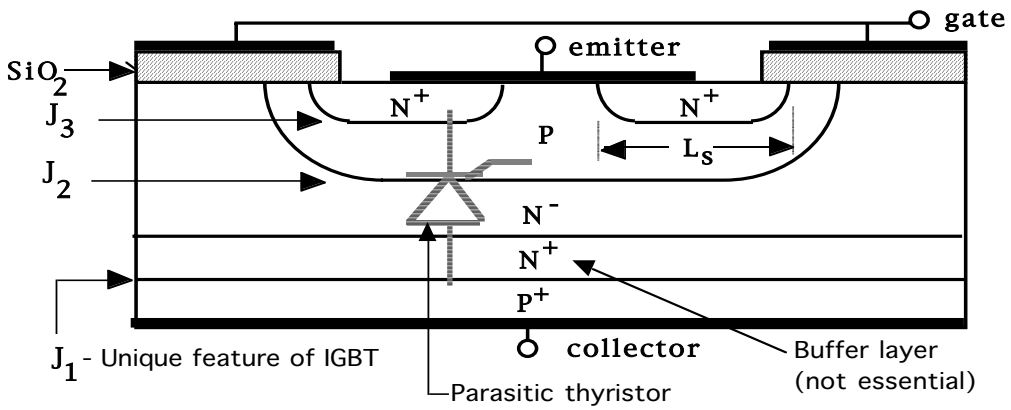


- Punch-thru IGBT

IGBT I-V Characteristics and Circuit Symbols

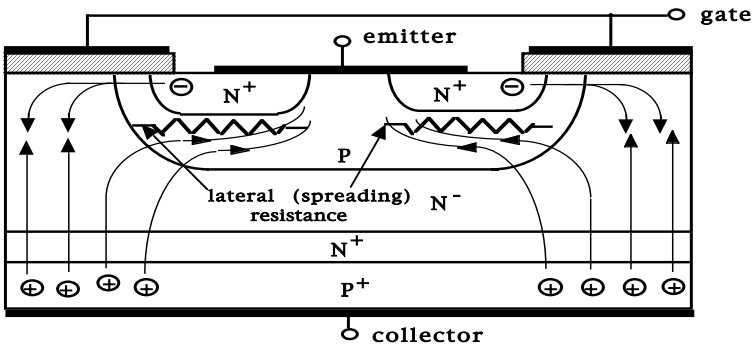


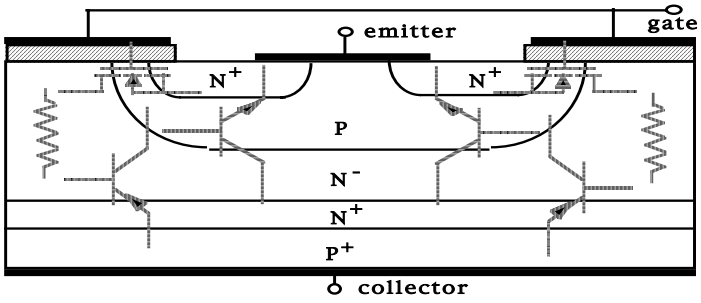
Blocking (Off) State Operation of IGBT



- Blocking state operation - $V_{GE} < V_{GE(th)}$
- Junction J_2 is blocking junction - n^+ drift region holds depletion layer of blocking junction.
- Without N^+ buffer layer, IGBT has large reverse blocking capability - so-called symmetric IGBT
- With N^+ buffer layer, junction J_1 has small breakdownvoltage and thus IGBT has little reverse blocking capability - anti-symmetric IGBT
- Buffer layer speeds up device turn-off

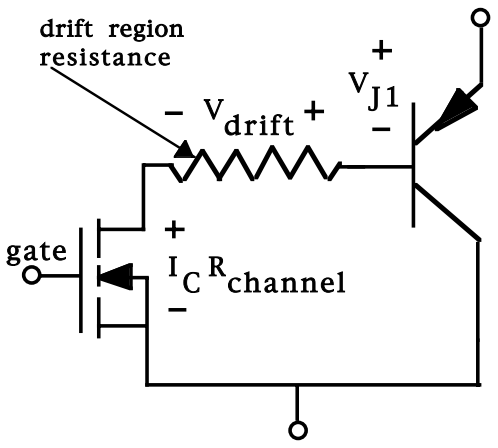
IGBT On-state Operation

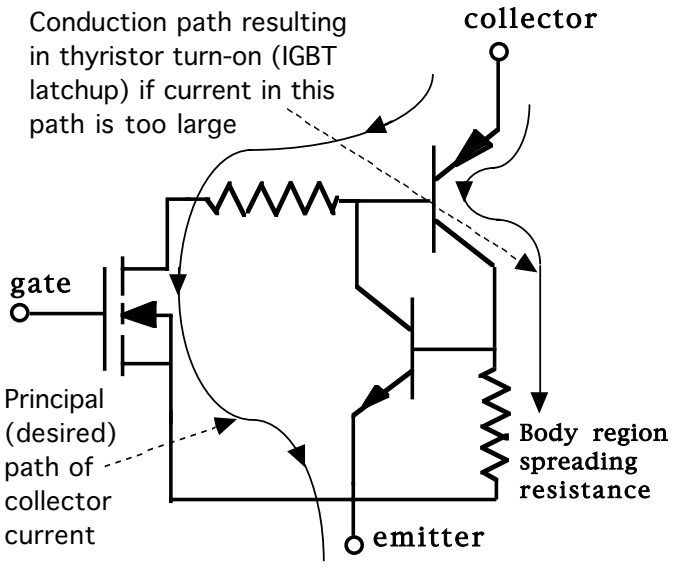




- MOSFET section designed to carry most of the IGBT collector current
- On-state $V_{CE(on)} = V_{J1} + V_{drift} + I_C R_{channel}$
- Hole injection into drift region from J_1 minimizes V_{drift}.

Approximate Equivalent Circuits for IGBTs

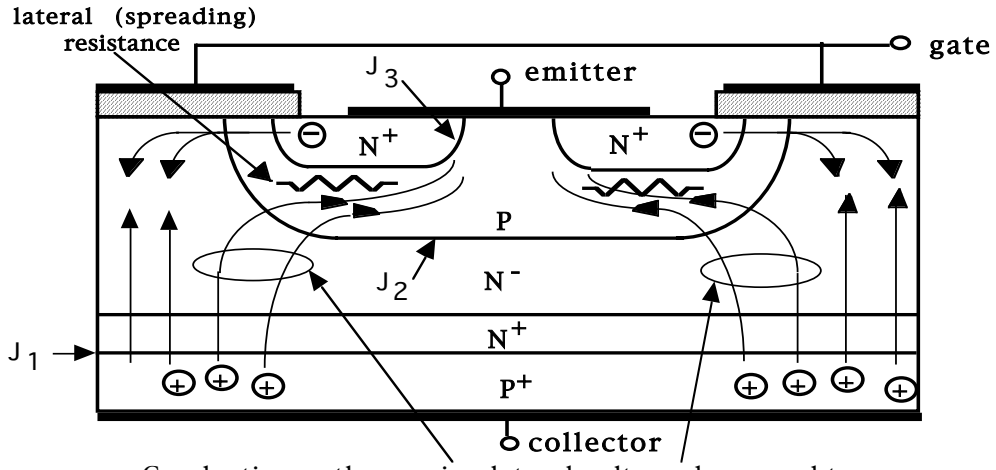




- Approximate equivalent circuit for IGBT valid for normal operating conditions.
- $V_{CE(on)} = V_{J1} + V_{drift} + I_C R_{channel}$

• IGBT equivalent circuit showing transistors comprising the parasitic thyristor.

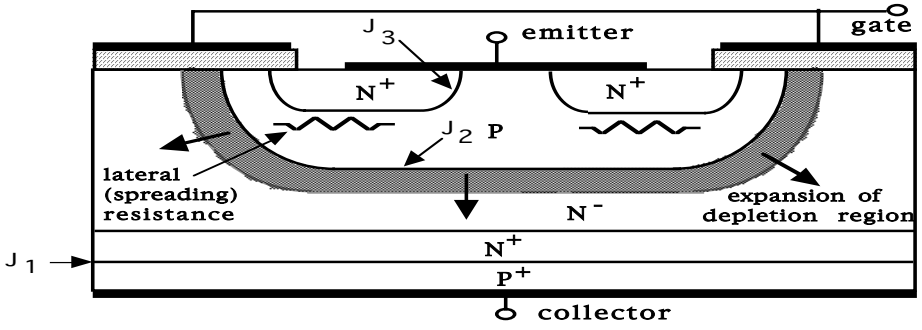
Static Latchup of IGBTs



Conduction paths causing lateral voltage drops and turn-on of parasitic thyristor if current in this path is too large

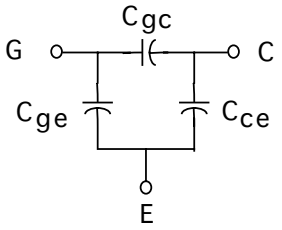
- Lateral voltage drops, if too large, will forward bias junction J3.
- Parasitic npn BJT will be turned on, thus completing turn-on of parasitic thyristor.
- Large power dissipation in latchup will destroy IGBT unless terminated quickly. External circuit must terminate latchup - no gate control in latchup.

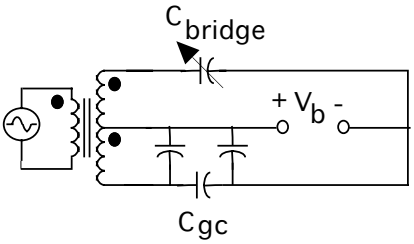
Dynamic Latchup Mechanism in IGBTs



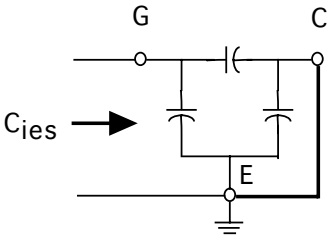
- MOSFET section turns off rapidly and depletion layer of junction J2 expands rapidly into N^- layer, the base region of the pnp BJT.
- Expansion of depletion layer reduces base width of pnp BJT and its a increases.
- More injected holes survive traversal of drift region and become “collected” at junction J2.
- Increased pnp BJT collector current increases lateral voltage drop in p-base of npn BJT and latchup soon occurs.
- Manufacturers usually specify maximum allowable drain current on basis of dynamic latchup.

Internal Capacitances Vs Spec Sheet Capacitances

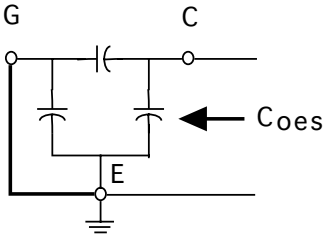




Bridge balanced (Vb=0) Cbridge = $C_{gc} = C_{res}$



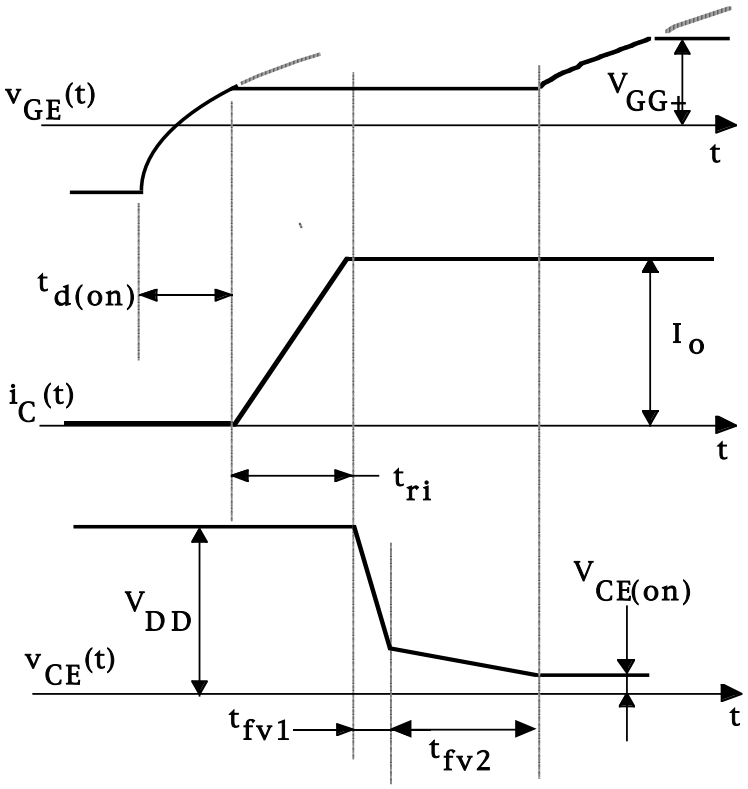
$C_{ies} = C_{ge} + C_{gc}$



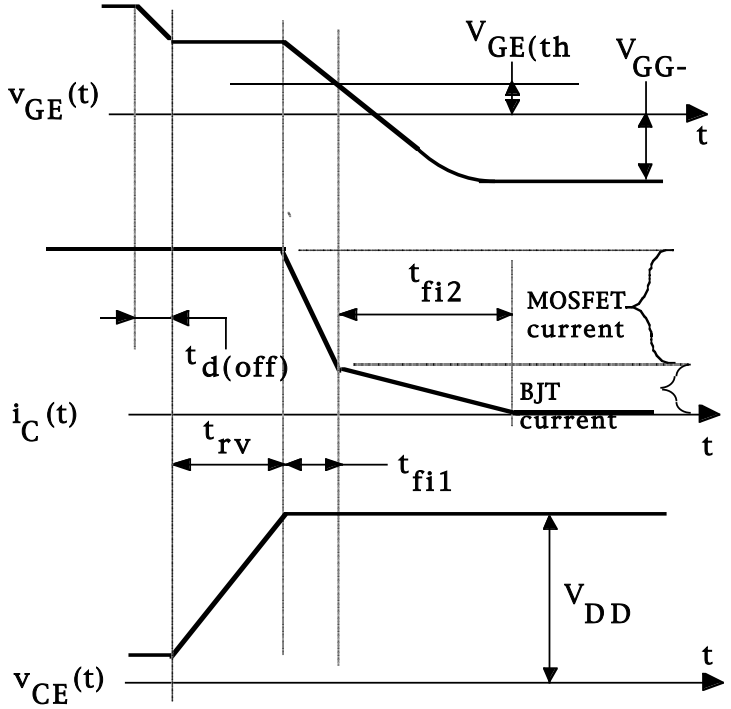
$C_{oes} = C_{gc} + C_{ce}$

IGBT Turn-on Waveforms

- Turn-on waveforms for IGBT embedded in a stepdown converter.
- Very similar to turn-on waveforms of MOSFETs.
- Contributions to t_{vf2}.
  - Increase in C_{ge} of MOSFET section at low collector-emitter voltages.
  - Slower turn-on of pnp BJT section.

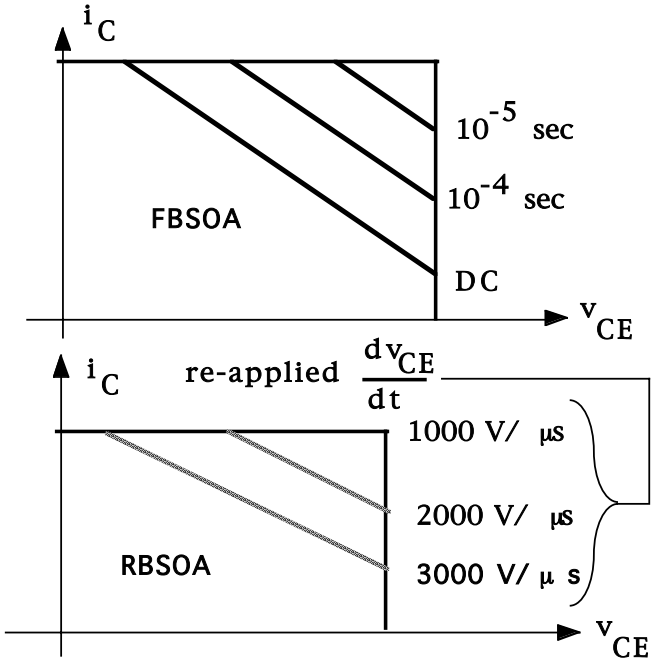


IGBT Turn-off Waveforms



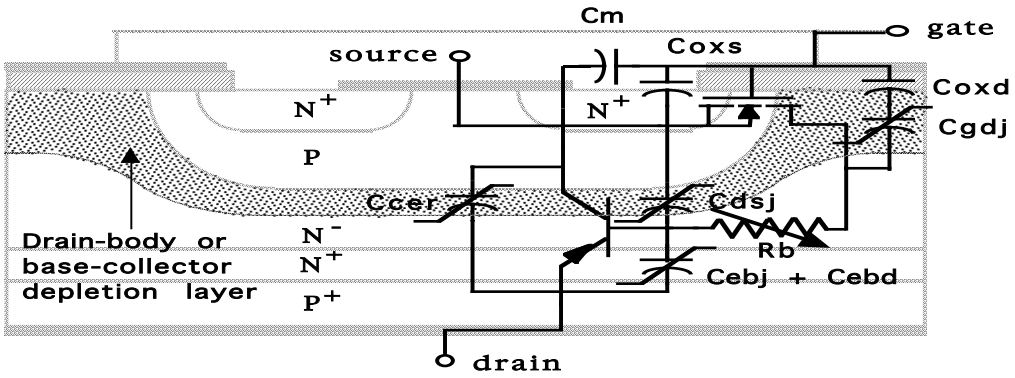
- Turn-off waveforms for IGBT embedded in a stepdown converter.
- Current "tailing" (t_{fi2}) due to stored charge trapped in drift region (base of pnp BJT) by rapid turn-off of MOSFET section.
- Shorten tailing interval by either reducing carrier lifetime or by putting N^+ buffer layer adjacent to injecting P^+ layer at drain.
- Buffer layer acts as a sink for excess holes otherwise trapped in drift region becasue lifetime in buffer layer can be made small without effecting on-state losses - buffer layer thin compared to drift region.

IGBT Safe Operating Area



- Maximum collector-emitter voltages set by breakdown voltage of pnp transistor - 2500 v devices available.
- Maximum collector current set by latchup considerations - 100 A devices can conduct 1000 A for 10 μsec and still turn-off via gate control.
- Maximum junction temp. = 150 C.
- Manufacturer specifies a maximum rate of increase of re-applied collector-emitter voltage in order to avoid latchup.

Development of PSpice IGBT Model

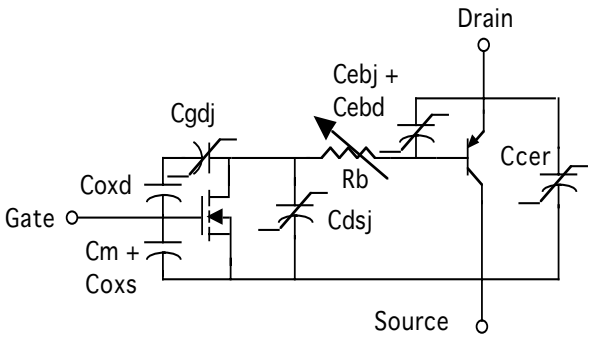


- Nonlinear capacitors Cdsj and Ccer due to N^-P junction depletion layer.
- Nonlinear capacitor Cebj + Cebd due to P^+N^+ junction
- MOSFET and PNP BJT are intrinsic (no parasitics) devices
- Nonlinear resistor Rb due to conductivity modulation of N^- drain drift region of MOSFET portion.
- Nonlinear capacitor Cgdj due to depletion region of drain-body junction (N^-P junction).
- Circuit model assumes that latchup does not occur and parasitic thyristor does not turn.

• Reference - "An Experimentally Verified IGBT Model Implemented in the SABER Circuit Simulator", Allen R. Hefner, Jr. and Daniel M. Diebolt, IEEE Trans. on Power Electronics, Vol. 9, No. 5, pp. 532-542, (Sept., 1994)

Parameter Estimation for PSpice IGBT Model

- Built-in IGBT model requires nine parameter values.
  - Parameters described in Help files of Parts utility program.
- Parts utility program guides users through parameter estimation process.
  - IGBT specification sheets provided by manufacturer provide sufficient informaiton for general purpose simulations.
  - Detailed accurate simulations, for example device dissipation studies, may require the user to carefully characterize the selected IGBTs.



- Built-in model does not model ultrafast IGBTs with buffer layers (punch-through IGBTs) or reverse free-wheeling diodes

PSpice IGBT - Simulation Vs Experiment